

Challenges and Promises of Reconfigurable Computing

Problems and Challenges

Hardware platforms

1. Loose coupling between microprocessor system and FPGA system
2. Applications constrained by the I/O Bandwidth, and the control transfer overhead
3. Long reconfiguration time and minimal support for partial reconfiguration in the current generation of FPGA devices

Tools

1. Lack of common high-level language capable of modeling both software and hardware
2. Long time of hardware synthesis and placing & routing compared to software compilers

Tools

3. Manual platform mapping, including
 - SW/HW partitioning
 - FPGA mapping
 - Data transfer & synchronization among FPGAs
 - SW/HW interface
 - Use of memories
 - Sequence of run-time reconfigurations

4. Limited portability of codes.
Close binding between platforms and software environments of each vendor

Applications

1. Limited range of applications and number of users
2. More library development needed
3. Choosing optimal design granularity for library components

Promises of the reconfigurable technology

- Several orders of magnitude speed-up for computationally intensive applications
- Large reduction in power consumption and cost of ownership
- Smaller size and less weight than traditional supercomputers
- More flexibility in types of functional units and operand sizes
- Can help overcome memory bottleneck